CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8) Applicant(s): Beintner et al.			Docket No. FIS920020080US2
Application No. 10/688,612	Filing Date October 17, 2003	Examiner A. Dink	Group Art Unit 2831

Invention: SELF-ALIGNED BURIED STRAP PROCESS USING DOPED HDP OXIDE

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10/688,612

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re divisional patent application of

Beintner et al.

Serial No.: Not yet assigned Group Art Unit: 2831

Filed: 10/17/2003 Examiner: A. Dink

For: SELF-ALIGNED BURIED STRAP PROCESS USING DOPED HDP

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits and calculation of the filing fee and further to the Amendment filed on October 17, 2003, please amend the above-identified application as follows:

IN THE CLAIMS:

1-11 (Cancelled).

12. (Original) A method of forming a memory device, said method comprising:

patterning a trench is a substrate;

filling a lower portion of said trench with a capacitor conductor;

forming a doped trench top oxide in said trench above said capacitor conductor; and

heating said structure to form a conductive buried strap in said substrate adjacent said trench top oxide.

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patterning a trench is a substrate;

filling a lower portion of said trench with a capacitor conductor;

forming a doped trench top oxide in said trench above said capacitor conductor; and

heating said structure to form a conductive buried strap in said substrate adjacent said trench top oxide.

13. (Original) The method in claim 12, wherein said process of depositing said doped trench top oxide comprises a high density plasma-chemical vapor deposition (HDP-CVD) process.

14. (Original) The method in claim 12, wherein said process of depositing said doped trench top oxide comprises the following parameters:

deposition rate of silane reactant gas flow 10 - 75 sccm;

approximate bias plasma power 300 B 1000 W; and

phosphine gas delivery at gas flows below 5 sccm.

15. (Original) The method in claim 12, wherein during said process of depositing said doped trench top oxide layer, a percentage by weight of dopant in said doped trench top oxide layer is less than 1%.

16. (Original) The method in claim 12, further comprising depositing an undoped trench top oxide in said trench above said doped trench top oxide.

17. (Original) The method in claim 16, further comprising depositing a gate conductor in said trench above said undoped trench top oxide layer, wherein said undoped trench top oxide layer insulates said gate conductor from said capacitor conductor.

18. (Original) A method of forming a memory device, said method comprising:

patterning a trench is a substrate;

filling a lower portion of said trench with a capacitor conductor; and

forming a trench top oxide in said trench above said capacitor conductor, wherein said forming of said trench top oxide includes depositing a doped trench top oxide layer above said capacitor conductor, and forming an undoped trench top oxide layer above said doped trench top oxide layer.

19. (Original) The method in claim 18, further comprising depositing a conductive node strap in said trench adjacent said capacitor conductor.

20. (Original) The method in claim 18, further comprising heating said structure to form a conductive buried strap in said substrate adjacent said trench top oxide.

21. (Original) The method in claim 18, wherein said process of depositing said doped trench top oxide layer comprises a high density plasma-chemical vapor deposition process.

22. (Original) The method in claim 18, wherein during said process of depositing said doped trench top oxide layer a percentage by weight of dopant in said doped trench top oxide layer is less than 1%.